## Remarks

In response to the Office Action mailed January 12, 2004, Applicants respectfully request reconsideration of the pending claims. To further prosecution of this application, Applicants submit the above amendments.

Claims 1, 2, 4, 7-18, 20-22, 32, 35, 36, 40-45, and 47-48 are currently active in the application. Claim 35 is objected to, claims 41, 45, and 47-48 are rejected as being indefinite under 35 U.S.C. §112, and claims 1, 2, 4, 7-18, 20-22, 32, 35, 36, 40-45, and 47-48 are rejected under 35 U.S.C. §103(a) as unpatentable over Gramann et al. (U.S. 5,701,151) in view of Mahulikar et al. (U.S. 5,629,835).

After addressing the objection and the rejections for indefiniteness, we discuss rejected independent claims 1, 14, 16, 21, 32, and 40 that have been amended to distinguish them over the cited art. These claims now require the silicon wafer and the single conductive region of the recess to be conductively coupled so as to be substantially at the same electrical potential and find support in Fig. 1 and on page 3, lines 8-9 ("The conductive region 17 covers all or a portion of the recess 14..."), page 4, line 25 ("To the recess is applied at least one layers of conductive material (210)."), and page 5, lines 5-6 ("The first layer is titanium followed by a layer of copper and a layer of chrome, which cover the contour of the recess and at least a portion of the top of the silicon wafer.").

Claim 45 has also been amended to distinguish over the cited art and now requires that the electronic component contain a die with first and second contacts. Conductive bonding material electrically couples the first contact to an electrically conductive region that electrically couples both the first contact and the wafer to an electrical input. Non-wire bonding couples the second contact to a second electrical input. Support for the

amendments to claim 45 may be found in Fig.1, on page 3, lines 8-9 ("conductive region 17 covers all or a portion of the recess 14..."), and on page 6, lines 6-7 ("...process does not require wire/tab bonding...").

**Claims 35, 41, 45, and 47-48 are now in allowable form.**

The informality attributed to claim 35 has been corrected. The indefiniteness attributed to claims 41 and 45, 47, and 48 has been addressed by amendment of claim 41 to require the "second conductive region" with antecedence in claim 10 and amendment of claim 45 to require "an electrically conductive region" with support on page 3 line 8 of the application.

**Claims 1, 14, 16, 21, 22, 32, and 40 are allowable over the art of record.**

Claim 1 is directed to an electrical component having an electronic device package at least formed from an integral silicon wafer having a recess with a single conductive region, a bare die electronic device disposed in the recess, and a dielectric material disposed to form a planar surface over the recess. In addition, claim 1 requires conductive coupling of the silicon wafer and the single conductive region so that they are at substantially the same electrical potential. In contrast, Gramann et al. describes a package where there is no common electrical potential between a carrier plate and a conductor lying within a recess of the carrier plate and where there is more than a single conductor lying within the recess.

Gramann et al. describe an optoelectronic transducer where either the carrier plate is an electrical insulator or an electrical conductor coated with an insulating layer. (See

Gramann et al., column 5, line 64-column 6, line 9.) Two mutually separate electrically conductive terminal tracks are applied to a bottom floor and to the sides or walls of the recess. (Column 5, lines 42-45.)

Whether an insulator or an insulated conductor, the carrier plate does not share electrical potential with the terminal tracks. Gramann et al. categorizes silicon as an insulator. However, even if silicon is regarded as a conductor and not as an insulator, Gramann et al. does not anticipate the first element of claim 1. Gramann et al. requires two electrical tracks, not a single conductive region, to lie within the recess and operation of the optoelectronic transducer requires that the two terminal areas be connected to two different electrical inputs.

Mahulikar et al. describe a metal ball grill array package where a semiconductor device is bonded to a heat spreader by a suitable die attach material where the heat spreader is electrically isolated by a surrounding polymer. (See Mahulikar et al., Fig. 6.) The device may also be mounted on a base, that, if not electrically insulating, is given an electrically insulating coating. (See Mahulikar et al., Fig. 9 and column 6, lines 55-57.) In no case is electrical contact made between the device and the base.

Mahulikar et al. does not satisfy the requirements of claim 1 either alone or in combination with Gramann et al.. Mahulikar et al. contains no teaching of a silicon wafer conductively coupled to a single conductive region. In Mahulikar et al., where a semiconductor device is bonded to a heat spreader with die attach material, the heat spreader is electrically isolated by epoxy, thereby preventing electrical connection. (See Mahulikar et al. column 5, line 63-column 6, line15 and Fig. 7.) Even where the semiconductor device is bound to a conducting base, the base is covered with electrically

insulating layer, preventing conductive coupling of the base to the heat spreader. (See Mahulikar et al. column 6, lines 50-57 and, Fig. 9-18).

Because limitations of a silicon wafer having a recess containing a single conductive region where the single conductive region is conductively coupled to the wafer so that the wafer and the conductive region are at substantially the same electric potential are not taught or suggested by the art of record, claims 1, 14, 16, 21, 22, 32, and 40 as amended are allowable over the cited art and claims 2-13 and 41 dependent from claim 1, claim 15 dependent from claim 14, claims 17-18, 20, and 42 dependent from claim 16, claim 22 dependent from claim 21, and claims 35-36 and 43-44 dependent from claim 32 are allowable for at least the same reasons.

**Claim 45 is now allowable over the cited art.**

Claim 45 is directed to an electrical component having a silicon wafer with a recess containing a die with first and second contacts. Conductive bonding material attaches the die to the wafer and electrically couples the first contact to an electrically conductive region that electrically couples the wafer and the first contact to an electrical input. Non-wire bonding connects the second contact to a second electrical input.

Gramann et al. uses wire bonding connecting conductors (Figs. 1-11). As Gramann et al. illustrates, a terminal track always lies at a level below the topside contact (to the body). Only wire bonding can electrically connect the topside contact with the terminal track. Non wire bonding cannot accommodate this height differential.

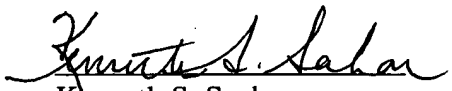
Furthermore, Mahulikar et al. also primarily employs bonding wire to connect contacts on the semiconductor device to the lead frame. Further, the flip chip alternative

of Figs. 16 and 17 is inconsistent with the requirement for conductive bonding material to electrically couple the wafer and a first device contact with an electrical input via an electrically conductive region. In Fig. 16, there can be no electrical coupling between a first contact and the wafer, as the base is electrically insulated. In Fig. 17, there can be no electrical coupling, because the support layer is necessarily insulating to maintain isolation between circuit traces. (See Mahulikar et al., column 10, lines 23-35.)

Because non wire bonding electrical coupling between a second contact and a second electrical input or electrical coupling between a first contact and a wafer is not taught or suggested by the art of record, claim 45 as amended is allowable over the cited art and claims 47 and 48 dependent from claim 45 are allowable for at least the same reasons.

In view of the foregoing amendments and remarks, this application is now in condition for allowance, and a notice to this effect is respectfully requested. If the Examiner believes, after these amendments, that the application is not in condition for allowance, the Examiner is invited to call the Applicants' attorney at the number listed below.

Respectfully submitted,



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